IN THE CLAIMS

Please amend the claims as follows.

1.-4. (Cancelled)

5. (Previously Presented) A capacitor comprising:

at least four conductive layers embedded in a dielectric, wherein the at least four conductive layers includes a first plurality of conductive layers interlaced with a second plurality of conductive layers; and

a plurality of vias coupling the at least four conductive layers to a plurality of connection sites on at least two surfaces of the capacitor, wherein the plurality of vias includes a first set of vias and a second set of vias, and the first set of vias couples the first plurality of conductive layers to a first plurality of connection sites on the at least two surfaces of the capacitor, and the first set of vias extends through openings in and is electrically isolated from the second plurality of conductive layers, and the second set of vias couples the second plurality of conductive layers to a second plurality of connection sites on the at least two surfaces, and the second set of vias extends through openings in and is electrically isolated from the first plurality of conductive layers, and wherein the plurality of vias are plated through holes.

6.-31. (Cancelled)

32. (Previously Presented) The capacitor of claim 5, wherein each of the at least four conductive layers comprises tungsten.

33. (Previously Presented) The capacitor of claim 5, wherein each of the at least four conductive layers comprises palladium.

34.-37. (Cancelled)

38. (New) The capacitor of claim 5, wherein at least one of the at least four conductive layers includes tungsten.

39. (New) The capacitor of claim 5, wherein at least one of the first plurality of conductive layers is fabricated from a paste that includes tungsten.

40. (New) The capacitor of claim 5, wherein at least one of the at least four conductive layers includes platinum.

41. (New) The capacitor of claim 5, wherein at least one of the at least four conductive layers includes palladium.

42. (New) The capacitor of claim 5, wherein the capacitor has a thickness of between about 0.5 millimeter and about 1 millimeter.

43. (New) The capacitor of claim 5, wherein the capacitor has a capacitance of between about 20 and about 30 microfarads.

44. (New) The capacitor of claim 5, wherein the first plurality of conductive layers is formed on a first dielectric sheet, and the second plurality of conductive layers is formed on a second dielectric sheet.

45. (New) The capacitor of claim 5, further comprising:

a pair of dielectric sheets formed from a material that includes barium titanate, for providing a pair of substantially rigid outer surfaces for the first plurality of conductive layers interlaced with the second plurality of conductive layers.

46. (New) The capacitor of claim 45, wherein each of the pair of dielectric sheets has a thickness greater than about 7 microns.

47. (New) The capacitor of claim 45, wherein each of the pair of substantially rigid outer surfaces has a plurality of connection sites operable for coupling the capacitor to a substrate using a controlled collapse chip connection (C4).

48. (New) The capacitor of claim 5, wherein the at least two surfaces is two surfaces.

49. (New) The capacitor of claim 5, further comprising:

a pair of substantially rigid outer surfaces formed from barium titanate; and

wherein the plurality of connection sites includes a plurality of pads located on the pair of substantially rigid outer surfaces, wherein at least two of the plurality of pads are capable of being coupled to a substrate using a solder bump, wherein the number of pads are coupled to the at least four conductive layers through the plurality of vias, and wherein the number of conductive layers is greater than about 50.

50. (New) The capacitor of claim 49, wherein the number of pads is greater than about 4000.